Experimental Demonstration of Four-Terminal Magnetic Logic Device with Separate Read- and Write-Paths

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Abstract

Magnetic logic has recently become an attractive candidate for future electronics. This paper describes the demonstration of a four-terminal spintronic device with distinct read- and write-paths ("mCell"). The mCell enables a non-volatile circuit technology (mLogic) with gain sufficient to drive fanout independent of CMOS [1]. Measured material properties and prototype device results are presented.

Introduction

Spintronics, where the spin polarization of electrons is exploited in computation, has been studied in recent years as a potential platform for logic circuit design. A number of approaches have been put forth that differ in design and implementation, but all tend to share the common thread that electron spin – not charge – is used to represent and transfer data. The magnetization direction of a bistable element generally stores the logic value, making the circuits non-volatile. Proposed technologies range from circuits based solely on dipolar coupling with no electrical signaling between gates [1]-[4] to devices and circuits based on the flow of pure spin currents [5].

Recently, we have proposed a magnetic logic technology ("mLogic") based on a current-driven four terminal device ("mCell") with isolated read- and write- paths [6],[7]. An input current pulse through the write-path switches its magnetic state, which is coupled through an electrically insulating magnetic material to the free layer of a magnetic tunnel junction (MTJ) with two reference layer pillars that constitute the read path. These devices can be configured into circuits based on current steering that require no tight CMOS integration and can operate on low, noisy supply voltages.

mCell Device and Circuits

The mCell (Fig. 1) is programmed by moving a domain wall (DW) with a current through the write-path of a magnetic nanowire by the spin Hall effect (SHE) [9]-[11]. This magnetization state couples to a free layer in the read-path through an electrically insulating magnetic material, causing the magnetization in each layer to align. The free layer in combination with a tunnel barrier and reference layer forms a magnetic tunnel junction (MTJ) in the read path, setting the resistance of the device. The direction of current through the write-path determines which logic state the device enters. Micromagnetic simulation solving the Landau-Lifshitz-Gilbert equation [12] is used to explore device switching characteristics as a function of material properties, device size, and input stimuli. Fig. 2 shows the domain wall speed is roughly linear with write current density; for scaled devices, these speeds translate to 500 ps – 1 ns switching times. The absolute current scales linearly with device width, and is on the order of tens of microamperes (Fig. 3).

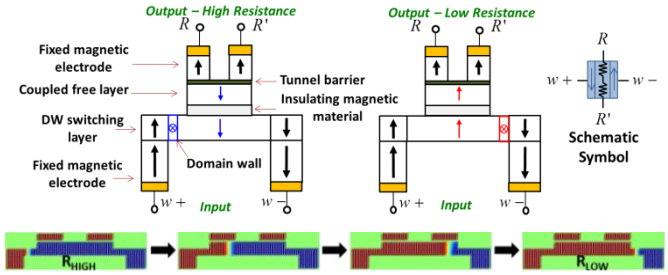

Fig. 1: (top left) Cross-section of mCell device with a write-path between (w^+,w^-) and a separate read-path between (R,R'); (top right) schematic symbol of mCell; (bottom) micromagnetic simulation of mCell SHE state switching.

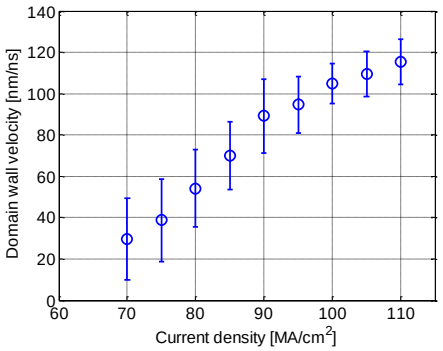

Fig. 2: Wall velocity increases roughly linearly with write current density.

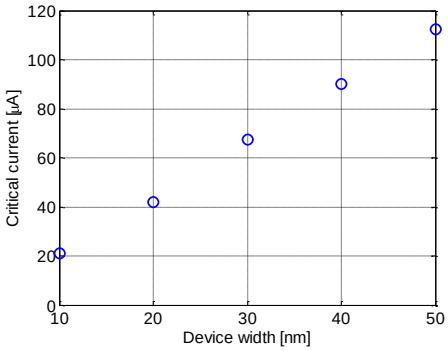

Fig. 3: Critical current scales linearly with device width.

The devices can be configured into circuits based on current steering, where the ratio of read-path resistances in one stage drives a positive or negative output current through

fanout mCells connected in series through their write-paths (Fig. 4). No integrated CMOS is required. Voltages of only ±100 mV or less are required to drive the required currents.

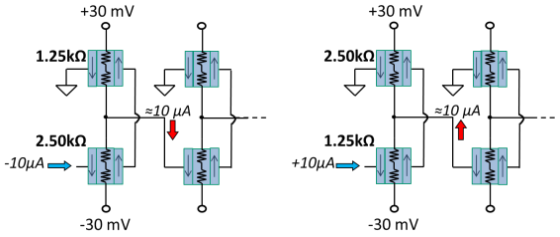

Fig. 4: Ratio of pull-up to pull-down mCell read-path resistance steers current into or out of series-connected write-paths of fanout mCells. The schematics show one inverter driving another.

mCells can also be used to design an all-magnetic MRAM bitcell (Fig. 5). The current flow through the write bitline (WBL) programs the inverter in the bitcell, which is used to isolate the third mCell (storage device) from other bitcells in an array. Driving the write wordlines (WWL+, WWL-) transfers the bit value to the storage cell based on current steering (Fig. 5). The cell is read by sensing the current along the read bitline (RBL) when the read wordline (RWL) is asserted. Current signaling enables low voltage (< 100 mV) operation and minimal energy loss in charging wordline and bitline parasitics. More details on mLogic can be found in [1].

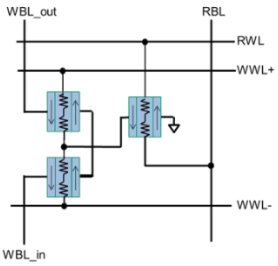

Fig. 5: Schematic of an all-magnetic mCell-based bitcell.

Materials Development

Individual mCell components were developed separately prior to integration in a single device. MTJs based on Ta/FeCoB/MgO/FeCoB/Ta (Fig. 6) were prepared by magnetron sputtering and subsequently annealed in a 4 kOe perpendicular field at 250-350°C resulting in a perpendicular tunneling magnetoresistance (TMR) up to 138% (Fig. 7) [13].

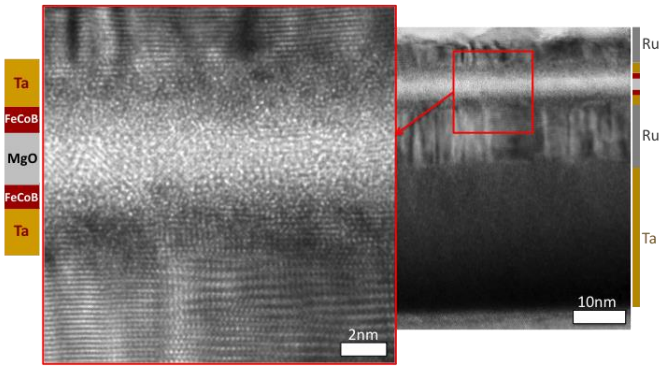

Fig. 6: Cross-sectional TEM image of MTJ films showing a smooth barrier.

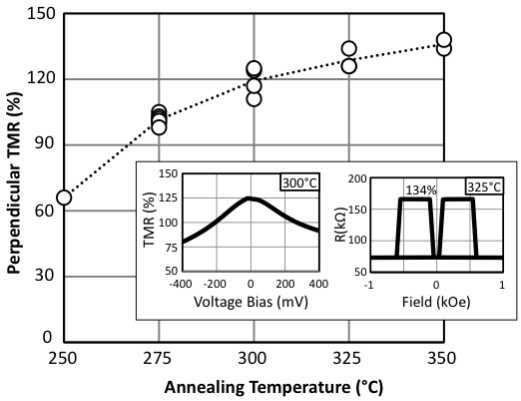

Fig. 7: TMR of 138% achieved with annealing stability up to 350 °C in Ta/FeCoB/MgO/FeCoB/Ta MTJs [13]. Inset: Bias voltage dependence and example R-H loop.

Fig. 8(a) shows Kerr images demonstrating domain wall motion (DWM) in a TaN(3nm) / Pt(2.5) / $[Co(0.2) / Ni(0.3)]_2$ / Co(0.2) / Ta(0.32) / TaN(6) wire in response to various current pulses. DWM is along the current direction, indicating the driving force is the SHE. No fields were applied. Velocity as a function of current density is plotted in Fig. 8(b). Each point represents an average of five pulses with error bars indicating the standard deviation. Various Ta cap layer thicknesses were tested due to the effect Ta has on the chirality of the DW. SHE driven wall motion requires that the domain wall have some Néel character. This can be realized through the Dzyaloshinskii-Moriya interaction (DMI) from the seed and capping layers. As the DMI term for Ta/Co and Pt/Co have the same sign [9], they will have a canceling effect on the wall character when on opposite sides. As such, we observe that limiting the Ta thickness improves DW velocity, with a maximum value of 125 m/s in the experiment (Fig. 9).

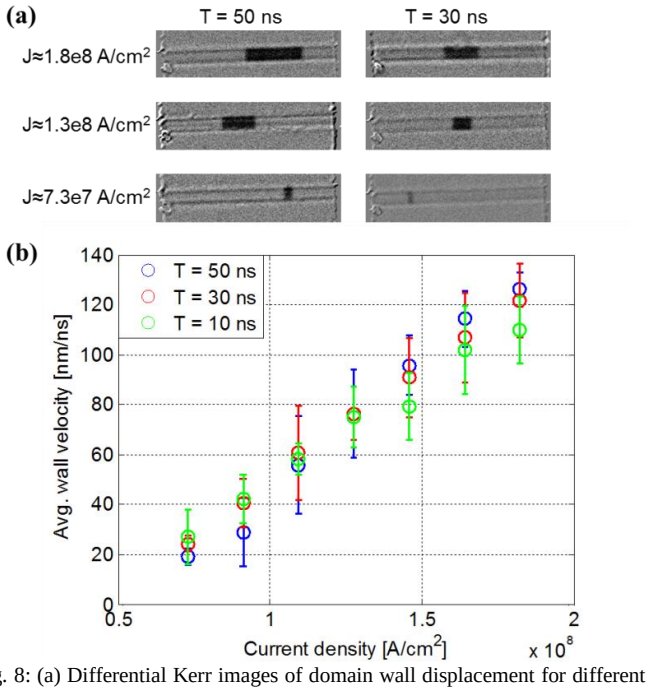

Fig. 8: (a) Differential Kerr images of domain wall displacement for different current densities and pulse widths; (b) Mean wall velocity increases linearly as a function of current density.

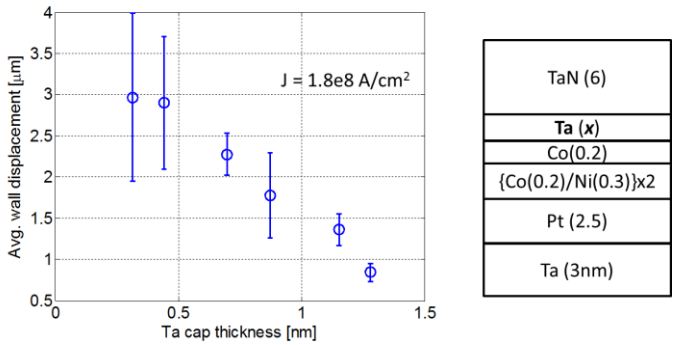

Fig. 9: Average domain wall displacement vs. Ta thickness in TaN(3nm)/Pt(2.5)/[Co(0.2)/Ni(0.3)]$_2$/Co(0.2)/ Ta(t_{Ta})/TaN(6) nanowires.

The magnetic oxide (coupling, insulating interlayer) was prepared by allowing a native oxide to form on metallic FeCoB in a 0.2 mTorr oxygen atmosphere. The FeCoB passivates, forming an electrically insulating, magnetic oxide layer of ≈1 nm (Fig. 10), similar to that observed in metal FeCo [14]. It has been shown that a 0.5 nm layer of Ta will not break coupling while still supporting DWM in the Co/Ni based write-path and necessary properties in the MTJ [15]. Coupling through the DW nanowire, magnetic oxide, and MTJ free layer was evaluated using the film stack of Fig. 11(a). At least 1 nm of oxide can maintain perpendicular magnetization due to coupling from the MTJ free layer and DW nanowire. This stack includes every layer of a full mCell device except for the top MTJ electrode.

Device Prototype

Based on the results of the developmental work, a prototype mCell with an integrated write- and read-path was fabricated using a combination of e-beam and optical lithography, RIE, and ion milling. The magnetic oxide was replaced by 0.5 nm of Ta in the prototype device to reduce fabrication complexity, meaning read- and write-paths are distinct and coupled but not electrically isolated. The full stack structure is seen in Fig. 12, which was post-annealed at 250°C. The films were annealed at 250°C to preserve DW motion, also resulting in low TMR values.

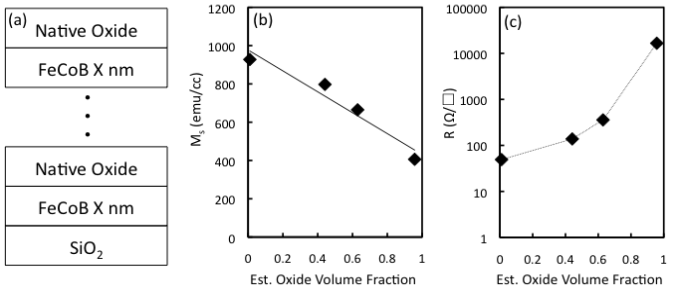

Fig. 10: (a) [FeCoB/NativeOxide]$_N$ multi-layers to characterize properties of oxidized FeCoB. Saturation magnetization (b) decays to 400 emu/cm^3 and sheet resistance (c) increases by three orders of magnitude as oxide volume fraction approaches 100%.

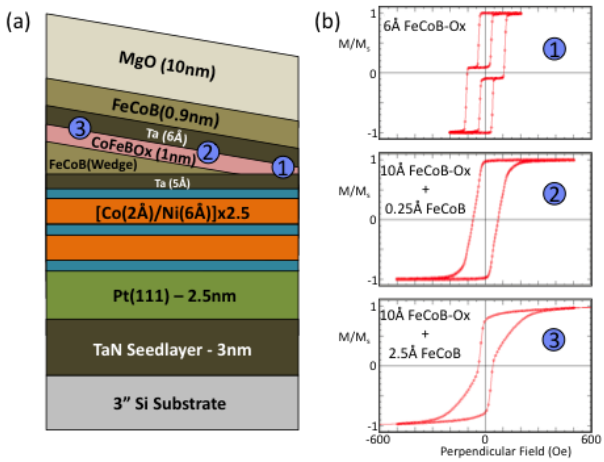

Fig. 11: (a) Film stack used to evaluate coupling within write-path. (b) Variation in M-H loops for different thicknesses of the spacer material (as listed). Full perpendicular remanence is observed for a 1nm FeCoB-oxide spacer layer.

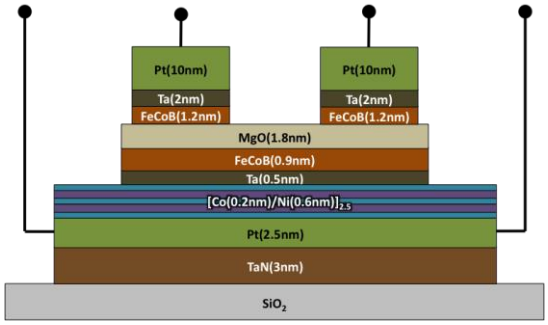

Fig. 12: Schematic stack structure of the prototype mCell.

The devices were patterned to be 1 μm wide and 10 μm long, with 275 nm of space between the two MTJs in the read-path (see plan view SEM and cross-sectional TEM images in Fig. 13(a) and (b)). A high resolution cross-sectional TEM micrograph is given in Fig. 13(c), showing the layer breakdown in the device. A current passed through the side lead of Fig. 13(a) (left of the image) is used to nucleate a DW in the locality of the lead by generation of a circulating Oersted field.

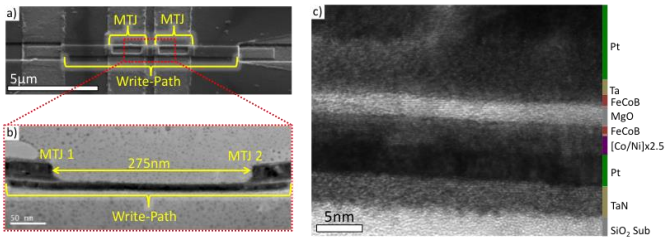

Fig. 13: (a) Plan view SEM image of fabricated device; (b) cross-sectional TEM image of device showing separation of read-path MTJs; (c) high resolution cross-sectional TEM image of device.

Current pulses injected in the write-path move the DW along the current flow by the SHE. Fig. 14 shows the location of the DW and corresponding resistance states in the structure. Polar Kerr microscopy images as well as micromagnetic

simulations of the DW location are shown for clarity. Initially, the DW is "outside" the MTJs (region 1, low resistance). A current pulse is injected, bringing the DW to the middle of the device (region 2, midpoint resistance). A bias field of roughly 50 Oe was required to overcome the energy barrier necessary to bring the DW out of its low energy position, due in part to magnetostatic interaction between the read-path free layer and reference layer. A subsequent current pulse brings the DW to the other end of the device (region 3, high resistance). The electrical measurement shown in the figure demonstrates the fundamental concept of the mCell, that by moving a DW with current in the write-path, the read-path resistance can be switched from a low state to a high state (or vice versa) via magnetic coupling.

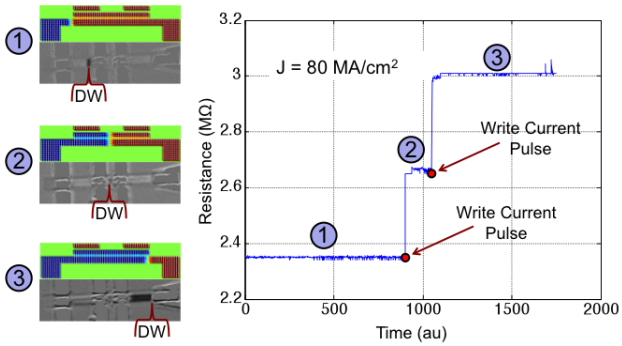

Fig. 14: Read-path resistance changes as the domain wall in the write-path is moved along with current. The resistance hits a midpoint when the wall is between the MTJs and increases to its maximum value when the wall moves under the second MTJ. Micromagnetic and Kerr images shown for domain wall location reference.

Higher current densities can be applied to ensure a single pulse can be used to switch the device (Fig. 15). Fig. 16 demonstrates the device can be reliably switched between high (low) states when negative (positive) current pulses are applied.

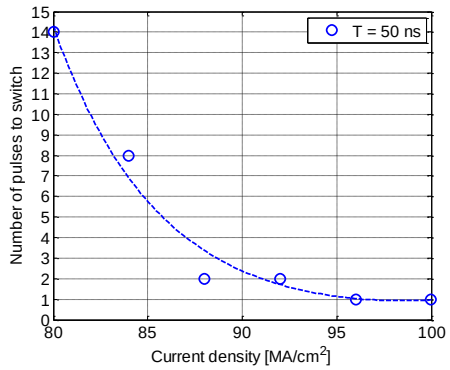

Fig. 15: Fewer pulses are required to switch the device as the write current density increases.

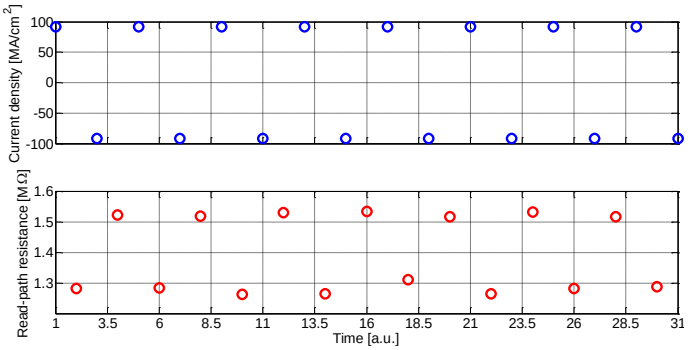

Fig. 16: Positive current pulses bring the device into a low resistance state and negative current pulses bring the device to a high resistance state.

Conclusion

The mCell is a device that could enable all-magnetic circuits and memory for non-volatile electronics. A prototype demonstrates the basic concept of the device, that a write-path current can digitally switch a separate read-path. Measured results of constituent components indicate suitable properties for the devices. Future work will involve integrating the magnetic oxide and improving the MTJ properties as means to enable fanout and the full realization of mLogic circuits.

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